FLASH MEMORY TECHNOLOGY FOR SPACE APPLICATION - AN APPROACH

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Abstract

Recently, flash memory technology has been considered for space application. This paper provides an approach for induction of the flash memory based mass data storage system to space program. It also, provides the studies and experiments that have been carried out in recent past to understand and characterize the behavior of flash memory in space environment. Further, it provides the design aspects which need to be addressed when dealing with flash memory for space environment, as identified by domain experts.

Keywords: Bit Error Rate, DRAM Chips, Flash Memories, Error Correction Codes, Satellites

Introduction

Initially, a simple sequential tape recorder was used as storage technology for mass data storage in space systems. Henceforth, Memory technology for space application is evolving as in commercial application. The evolution is driven by the requirements coming from the complex space mission and the emerging memory technology for commercial application. For more than a decade, DRAM technology devices are in use for mass storage in space systems [1].

Flash memory technology is being used for mass data storage in the consumer electronics products [2]. Recent past, Flash memory technology is being considered for space application for their non volatile, high storage density, low power, and high data throughput [1]. Towards this, experiments have been conducted to study the impact of particle radiation on performance of flash memory devices. Also, the challenges in adopting the flash memory technology for space applications have been studies by domain experts.

This paper aims to provide an overview of the flash memory technology, conclusion of the experiments conducted on flash memory technology in recent time to study the impact of particle radiation, design parameters of flash memory which need to be critically looked into, for space application, as identified by domain experts. It also provides, the approach for induction of the flash memory based mass data storage system to space program.

Flash Memory Technology

Flash memories store data as charge trapped on a floating gate between the control gate and the channel of a CMOS transistor. The basic structure of a flash-memory cell uses a dual sandwiched gate structure, interposing a floating gate between the body of the device and the control gate. It is similar to the structure of an EEPROM. Compared to EEPROM, Flash memory technology uses a much thinner oxide between the floating gate and channel region. The thin oxide allows charge to be transferred to and from the floating gate by either of two mechanisms namely FowLer-Nordheim(F-N) tunneling from the source or body, or hot-electron injection from the channel region [3].

NOR and NAND are the two basic structures that are used for the development of flash-memory. The NOR
structure, shown in Fig.1, provides direct access to individual cells, but increases cell area because of the need for contacts at each drain and source connection [4].

The NAND structure, shown in Fig.2, is more compact because it does not provide contacts to individual source and drain regions. But, cells in the NAND structure require reading and writing through the other cells in the stack. This results in inherently slower cell access [4].

A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations of the flash memory. Reading can be done relatively rapidly for either cell architecture. However, erasing and writing are very slow operations compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks and erasing and writing operations are done at the block level [4]. NAND flash memory is preferred for storage systems due to the very high memory capacity per device.

To evaluate the flash memories, it is essential to identify the operating modes of the device for a particular application. Flash memories can be operated in five basic modes as given below [3].

- Unpowered mode, which only applies power during the relatively short duration when the memory contents are used.
- Powered standby mode, in which the device is ready to begin reading, but the address lines are static.
- A read-only mode, which applies continuous power to the device, along with address, clock and control sequences for reading, but never applies power to the write circuitry.
- A read-mostly mode, or powered static mode, which is similar to the previous mode, but applies voltage to the charge pump and may also include brief periods for active writing.
- A mixed read and write mode (Erase-Write-Read (EWR) mode), which involves many, write cycles so that write duty cycle is a significant fraction of the total period.

New design techniques such as multilevel storage have been developed to increase storage density in flash memory. Thus, each gate can store one or more bits of information depending on whether it is a Single-Level Cell (SLC) or a Multi-Level Cell (MLC).

Further, the complexity of the device increases with reduction in the cell size. Because of its complexity, flash memories cannot be considered as simple memory device. So, it is quite interesting to determine how they respond in a radiation environments.

**Radiation Effects, Single Event Effect and Bit Error Rate**

In the past, experiments were conducted on flash memory to understand the impact of Total Ionizing Dose (TID) and Single Event Effects (SEE). Also, its performance was verified with respect to bit error rate, during the experiments.

Many of the heavy-ion tests were done with the device in a static mode during the irradiation period. This simulates a very low duty cycle read-only mode and eliminates the possibility that the upset in the decoding or write logic might interfere with cell upset during active-reads. Reading the memory contents after the irradiation test, provides a direct way to determine whether portions of the memory were changed during irradiation. Some tests were also done in EWR mode. Tests were also done with devices unpowered to determine whether heavy ions could introduce cell upsets or operational error in unpowered devices [3].

**Details About the Results of One of the Radiation Test Reported**

Way back, a radiation test was conducted on flash memory from Intel and Samsung devices and its results were reported [4]. The details about the experiments are provided below in brief.

Two Intel devices that use multi-level NOR flash architecture were selected for above radiation testing namely 28F320 (32Mb) and 28F640 (64Mb). Both parts operate with a 5-volt external power supply and an internal charge pump is used to generate the higher voltage required to erase and write the memory, typically 12 V. A Samsung 128Mb device, KM29U128, was also selected for radiation testing to compare the two architectures. The Samsung device uses a 3.3V power supply. It also uses an internal charge pump. Higher voltages are required for erasing and writing, typically 20V [4].
Total Ionizing Dose (TID)

Total dose tests were done using the JPL cobalt-60 test facility at either of two dose rates: 25 rad (Si)/s and 0.012 rad (Si)/s using a series of stepped irradiations. Measurements were made after each irradiation step with an advanced test system. The complex patterns were used for the comprehensive functionality check which is capable of detecting address or decoding errors.

The result of read mode for Intel 32MB-multilevel device, had indicated marginal increase in the standby current during irradiation. The device would no longer function after the second irradiation level [12 k rad (Si)]. When tested without bias, the device continued to operate at higher levels. After 16 k rad (Si) approximately 3,500 bits failed (a small fraction of the total number of bits).

The 64-Mb multi-level Intel flash memory behaved differently. The standby current increased much more rapidly with increasing radiation levels when bias was applied compared to results for the 32-Mb devices. The 64-Mb devices typically operated to levels well above 20 k rad (Si). Failure occurred in only a small number of cell locations even though the power supply current increased by more than an order of magnitude. When tested without bias, the 64-Mb devices passed read functionality up to 50 k rad (Si) and showed only slight increases in standby current. However, at 75 k rad (Si) a large number of addressing errors occurred.

Test results for the 64-Mb Intel device in the fully operational mode (EWR) were different from the READ mode. When irradiations were carried out under bias, the device became fully nonfunctional at 11 k rad (Si), where as the device continued to operate with only a few errors during tests in "read" mode. Without bias, the device also failed at much lower levels when fully operational tests were done between irradiations. Small numbers of write errors occurred between 30 and 40 k rad (Si).

For the 128-Mb Samsung devices, with biased irradiation, the standby current increased by several order of magnitude at about 20 k rad (Si). When tested without bias, the device functioned to levels above 100 k rad (Si) with only a small number of "read" errors. Errors of this type could be easily accommodated with basic error detection- and-correction techniques.

For the 128-Mb Samsung devices, with full functionality tests between successive irradiation levels, erase-mode failures were observed at 8 k rad (Si) under bias irradiation, in EWR(Erase-Write-Read) Mode. Older technology devices from Samsung behaved quite similar when tested in this mode, failing in E/W/R mode at approximately 10 k rad (Si) [4]. This corresponded closely with the total dose level where the standby current started to increase. When fully functional tests were done on devices that were unbiased during irradiation, erase failures occurred at 45 k rad (Si).

Earlier work [4] indicated that charge pump as the weak link. The effect of ionizing dose was to shift the threshold and reduce Vout of the charge pump. Any stage-to-stage increases in leakage would also reduce the charge pump output. Additionally, output drops rapidly as current demand increases. The increases in standby current on the devices mean a different failure mechanism is dominant.

Single Event Effect and Bit Error Rate

Single event testing was done at Brookhaven National Laboratory using several different ion species. The range of the ions exceeded 38 µm in all cases. Errors did not occur in individual memory cells in the 128-Mb Samsung devices. However, the heavy ions caused functional operation that was consistent with upset in the controller or registers. The cross section for these errors was relatively small, on the order of 10^6 cm^2. Additionally, address upsets were observed during sequential access. Upsets of the page buffer were observed when reading the part during irradiation. They are dependent on the operating frequency and ion flux used for the irradiation run. In this case the device was tested by dynamically reading the contents of the memory at an access rate of approximately 3 MHz, with a flux of ~ 10^6 ions/cm^2-sec); these cause less than a 10% error in the measured cross sections. Only a few runs were made with irradiations while erasing or writing. During one such run with bromine with LET = 38, the device became unable to perform erasing. Inverting the fluence of this run gave a cross section estimate of 5 x 10^{-4} cm^2. This catastrophic result could be due to Single Event Gate Rupture (SEGR).

For the Intel multilevel flash devices, with all LETs, few functional errors were observed that were similar to the general types of errors observed for the Samsung devices. When high LET ions were used, read errors were observed. For example, with LET = 84 (iodine at a 45-degree angle of incidence) approximately 100 cell locations were stuck in a specific state, and could no longer be written. This could be caused by microdose errors [4] that
affect the sense amplifier detection threshold. The 32-Mb devices behaved similarly.

To summarize the outcome of the experiment reported, tests of multi-level flash memories have shown that they typically fail at relatively low levels, below 20 krad (Si), when biased during irradiation. The advanced devices tested in the experiment demonstrate lower failure levels relative to earlier generation devices. These devices undergo far less degradation when they are irradiated in an unbiased mode, and there are many applications where they can be used effectively in a mainly unpowered, read-only mode. However, they are far more vulnerable to failure in erase and write modes, which is probably caused by changes in the internal charge pump (erase and write functions required very high internal voltages). With relatively tight tolerances, Charge-pump failures were identified as the cause of failure at low total dose levels in older device type [4], where external erase/write voltages could be used instead of the internal charge pump. However, the newer devices do not provide this option. Single event upset in the newer devices appears to be similar to the older parts with some exceptions. Functional failures caused by cell upset in the very complex control and state registers used in flash memory architecture continue to occur. Catastrophic failures are still occurring for irradiations in EWR mode.

Details About the Results of Another Radiation Test Reported in the Past

Another experiment was conducted on another set of flash memory from Intel and Samsung and its results were reported [3]. The details about the experiments are provided below in brief.

Intel NOR flash memory devices namely 1Mb flash device 28F010, 16Mb flash device 28F016SA, 16Mb device 28F016SV were selected for the radiation test. From Samsung, 16 Mb NAND flash, KM29N16000 and 32Mb NAND flash, KM29N32000 were also included in the experiments.

Heavy ion tests were done with the device in static mode during irradiation period. Tests were also done with devices in unpowered condition and EWR modes. Two different radiation facilities were used, Texas A and M cyclotron and the brookhaven Van de graaff. Testing was done in vacuum, using ions with LET (Linear energy transfer) values from approximately from 7 to 60 MeV cm²/mg. certain tests were done up to 120 MeV cm²/mg.

Functional errors and memory upset were seen during the tests and they were recovering either with re-initialization or with power cycling. No stuck bits were seen for Intel devices. In addition to functional test, increase in current was also observed after the tests.

Test results for two Samsung devices were qualitatively very similar to Intel devices. Small number of permanent error was observed in 16 Mb Samsung devices but it is not observed for 32Mb devices.

To summarize the outcome of the experiment reported, test of these two flash memory technologies have shown that the single event upset effects are dominated by the complex architecture of these devices rather than upset in the storage array. The many operating conditions and functional upset conditions that occur, make it difficult to interpret-event upsets in flash memory. Recovery becomes more difficult because of the number of the functional errors that occur due to irradiation. Error correction would have to be implemented at the block level in order to correct for all of errors, along with power cycling to recover from modes that caused functional errors, but did not produce memory errors. The irradiation test indicates that cell upsets never occurred in unpowered devices, even for effective LET values up to 120 MeV·cm²/mg at a 60 degree angle [3].

Design Criteria for Space Application

Design of a solid state data recorder for space applications should address many constraints imposed by space environment. Hence, proper counter measures are needed to improve the dependability of the whole system. Designing flash memory based systems for space application requires exploring number of design dimensions to enhance reliability [5]. In recent time, use of flash memory in space systems is reported [1].

General observation is that unhardened commercial technology has variable radiation response, and requires testing for characterization. Also, Flash memories have bit error rate performance better than standard volatile memories, because of nonvolatile feature [6].

To start with, it is essential to assess the radiation tolerance requirements for a memory device, which is to be used in a data storage system of a spacecraft, and it depends on the location of the device, design of the spacecraft, orbit of the spacecraft and mission life [7]. Also, it is essential to know modes of operation of memory de-
vices and their frequencies in a mission life while designing the data storage system. Depending on the memory being selected, certain design techniques have to be adopted for reliable operation of a data storage system for space application.

To enhance the reliable operation of flash memory in space environment, certain design techniques have been indicated for space application by domain experts. Major design techniques are listed below.

First, up-screening is mandatory for the selected flash memory devices [1]. Since latch up is still an issue which can result in permanent failure for certain devices, there is a need to provide memory isolation feature when the situation demands and to increase memory failure tolerance.

Further, size of the blocks, number of pages for each block, data retention time and endurance are the other parameters of the flash which need to be considered while designing a system [8]. The manufacturer of the device will state these parameters in the data sheet.

Fault tolerance mechanisms shall be systematically applied to increase reliability and endurance of these devices [1]. In particular, redundancy must be built into the system to ensure data integrity during its operating lifetime.

Further, results of the radiation tests carried out on the selected devices needs to be studied to understand SEE error rates and patterns. In a case of absence of radiation test results, devices need to be fully characterized independently to understand its behavior to irradiation and to incorporate appropriate Error Correction Codes (ECC).

As per manufacturer and independent studies, flash memories have random failures. Hence, the common ECCs techniques of SDRAM such as simple Hamming codes cannot be directly applied to flash devices. Bose-Chaudhuri-Hocquenghem (BCH), Low Density Parity Check (LDPC), and so on may be a suitable choice [1]. Reed-Solomon codes were also indicated in the literatures [5]. Choosing the most suitable ECC for a specific mission is always a trade-off among design parameters.

Also, it has been experimentally verified that Single Event Functional Interrupts(SEFI) and Single Event Latchup (SEL) errors can be removed by reset or power cycling (i.e., switching off and on the memory) without any loss of data [1]. Hence, it is essential to provide local reset and power on/off features.

**Approach**

The approach for induction of the flash memory based mass storage system to space program can be as depicted in the Fig.3. The design and development of the flash memory based mass storage system start with the literature survey regarding the experiments that have been carried out in recent past to understand the behavior of flash memory in space environment. After the literature survey, suitable flash memory device will be identified for the application considering its electrical, thermal, packaging, assembly process and radiation tolerance specifications. The device from the established vendor will be considered while selecting the devices. As part of acceptance criteria, the selected device will be subjected to up-screening tests. Subsequently, specifications, quality aspects and up-screening test results of the selected device will be subjected to review process.

The next step in the activities is the design process. The design activities can start with the DRAM based mass storage system as the baseline configuration. The development of memory control logic for FLASH memory is the critical element of the design. The control logic circuit can be realized in a Field Programmable Gate Array (FPGA) device. The flash memory control logic and associated circuits need to be designed for space application considering the criteria indicated by the domain experts. The memory control logic needs to be built with mitigation techniques to overcome constraints imposed by space radiation. At the end of the design, the analysis will be carried out as part of the design activities. It includes functional, timing, power and thermal analysis of the system. The design analysis results will be subjected to review by peer committee.

After the review process, design verification model will be developed and tested to verify the implementation of the design. After successful completion of the design verification model tests, qualification model will be developed for design margin demonstration with respect to electrical, thermal and mechanical design specifications [7]. The qualification model will be subjected to series of electrical and environmental tests. The test levels will be higher than the expected for the system during storage, transportation, launch and on orbit. The qualification test levels include the margin over the expected level for the
hardware. Flight hardware fabrication process will start after successful completion of the qualification tests.

The flight model will be realized with those flash memory devices which have undergone up-screening tests. Later, the flight model will be subjected to series of acceptance tests at unit level prior to integrated test at spacecraft.

To begin with, flash memory can be attempted in small satellite program. On orbit performance of the flash memory based mass storage system needs to be monitored after launch. In addition to its on orbit performance, the adequacy of the mitigation techniques adopted in the design, needs to be assessed at regular interval. Based on its performance, necessary corrective measures need to be incorporated in the next version of the flight hardware. After successful induction of the flash based mass storage system to small satellite program, it can be attempted in other program too.

Conclusion

DRAM technology is very fast, reliable, and provides a very high data rate, but needs power back up to retain data. Flash technology has been considered for replacing the well-established DRAMs for their high storage density, low power, low cost, and high data throughput.

This paper provides details about the flash memory technology in brief, advantages and limitations of flash memory, outcome of the experiments conducted on flash memory technology in the past to study the impact of particle radiation, design parameters of flash memory which need to be considered for space application. The typical approach for induction of the flash memory based mass storage system to space program is also provided in this paper.

Flash memory intended for space application is available from established vendor. Radiation test data regarding TID and bit error rate at each radiation level will be provided along with the device by vendor. These data are maintained at the organization such as NASA, ESA, ISRO and data are available for reference. However, it becomes necessary to study the results of the radiation tests carried out on the selected devices to understand SEE error rates and patterns. It helps in incorporating appropriate design techniques to overcome the limitations. Same approach needs to be adopted when flash device of smaller size is adopted for the first time.

In general, coding has to be incorporated in the design to take care of soft error due to SEE. Further, the coding scheme needs to be selected such that it will be able to address both random and burst error. In addition to redundancy for memory, isolation feature needs to be incorporated in the design to take care of hard failure in the memory due to radiation. Further, independent ON/OFF switch needs to be provided to each group of flash memory or individual device to isolate the memory from the power supply when a need arises.

To conclude, flash memory appears to be the future semiconductor storage technology for mass storage in space systems provided suitable design techniques are adopted in the design. To begin with, flash memory can be attempted in small satellite program.

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**Fig.1 Cell Architecture of a NOR Flash Memory**

**Fig.2 Cell Architecture of a NAND Flash Memory Organised in 16-bit Stacks**
Fig. 3 Process Flow for Induction of Flash Memory Technology to Space Program